11. Fan-Out Packaging and Chiplet Heterogeneous Integration

Course Leader: John Lau – Unimicron

Course Description:

Fan-out wafer/panel-level packaging has been getting lots of traction since TSMC used their integrated fan-out to package the application processor chipset for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. Their future trends will also be explored. Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with varied sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented.

Course Outline:

1. Formation of FOWLP: (a) Chip-First (Face-Down), (b) Chip-First (Face-up), and (c) Chip-Last Fabrication of Redistribution Layers (RDLs) Formation of FOPLP: (a) Chip-First (Face-Down), (b) Chip-First (Face-Up), and (c) Chip-Last
2. TSMC InFO: (a) InFO-PoP, and (b) InFO-AiP Driven by 5G mmWave
3. Samsung PLP: (a) PoP for SmartWatches and (b) SiP SbS for Smartphones
4. Warpages: (a) Warpage Types and (b) Allowable Warpages
5. Reliability of FOWLP and FOPLP: (a) Thermal-Cycling and (b) Drop Course - Many Examples of FOWLP and FOPLP
6. Chiplet Design and Heterogeneous Integration (HI) Packaging vs. System-On-Chip (SoC) Advantages and Disadvantages of Chiplet Design and HI Packaging - Many Examples of Chiplet Design and HI Packaging
7. Chiplets Lateral Interconnects (Bridges) - Many Examples
8. Chiplet Design and HI Packaging on Organic Substrates (SiP) - Many Examples
9. Chiplet Design and HI Packaging on Silicon Substrates (TSV-Interposers) - Many Examples
10. Chiplet Design and HI Packaging on Fan-Out RDL Substrate - Many Examples
11. Assembly Technologies for Chiplet Design and HI Packaging

Who Should Attend:

If you are involved with any aspect of the electronics industry, you should attend this course. The lectures are based on the publications by many distinguished authors and the books (by the lecturer) such as Fan-Out Wafer-Level Packaging (Springer, 2018) and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023).

Bio: John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging and SMT assembly, has published more than 515 peer-reviewed papers (of which John is the principal investigator of 375 of those papers), holds 40 issued and pending US patents (25 of which john is the principal inventor), and 23 textbooks (John is the first author on all of these books). John has been actively participating to industry/academy/society meetings/conferences to learn, to share, and to contribute.